

FIG . 2

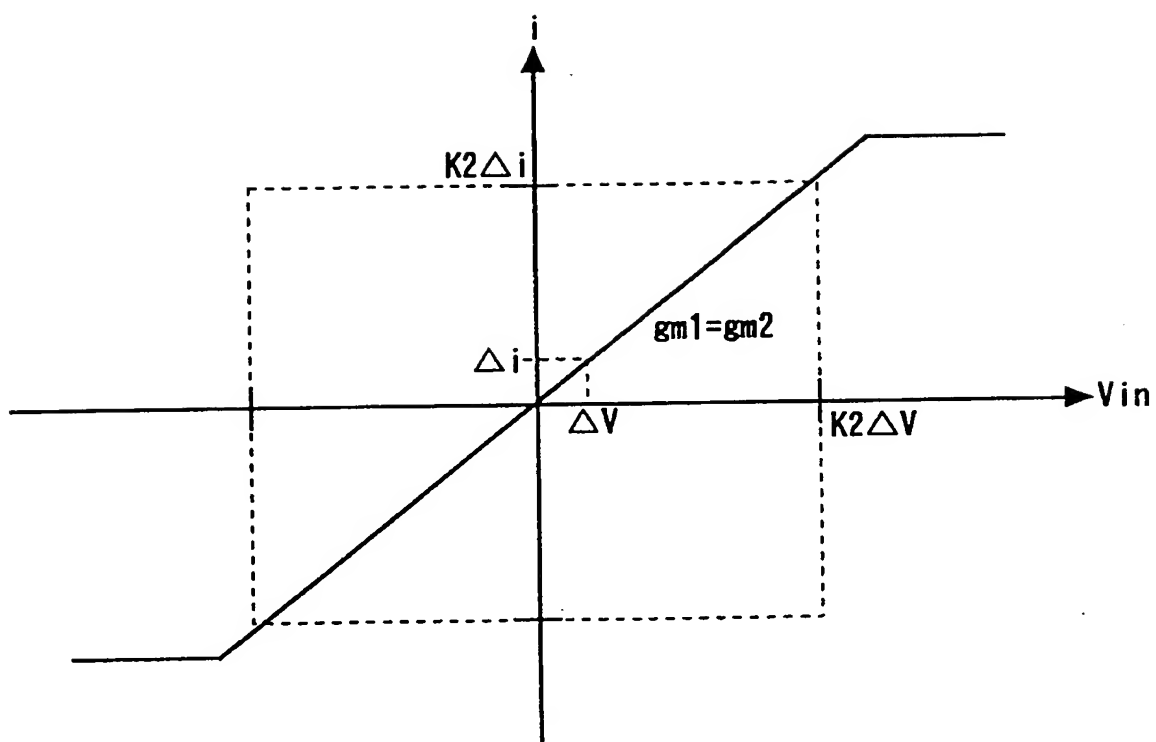


FIG . 3

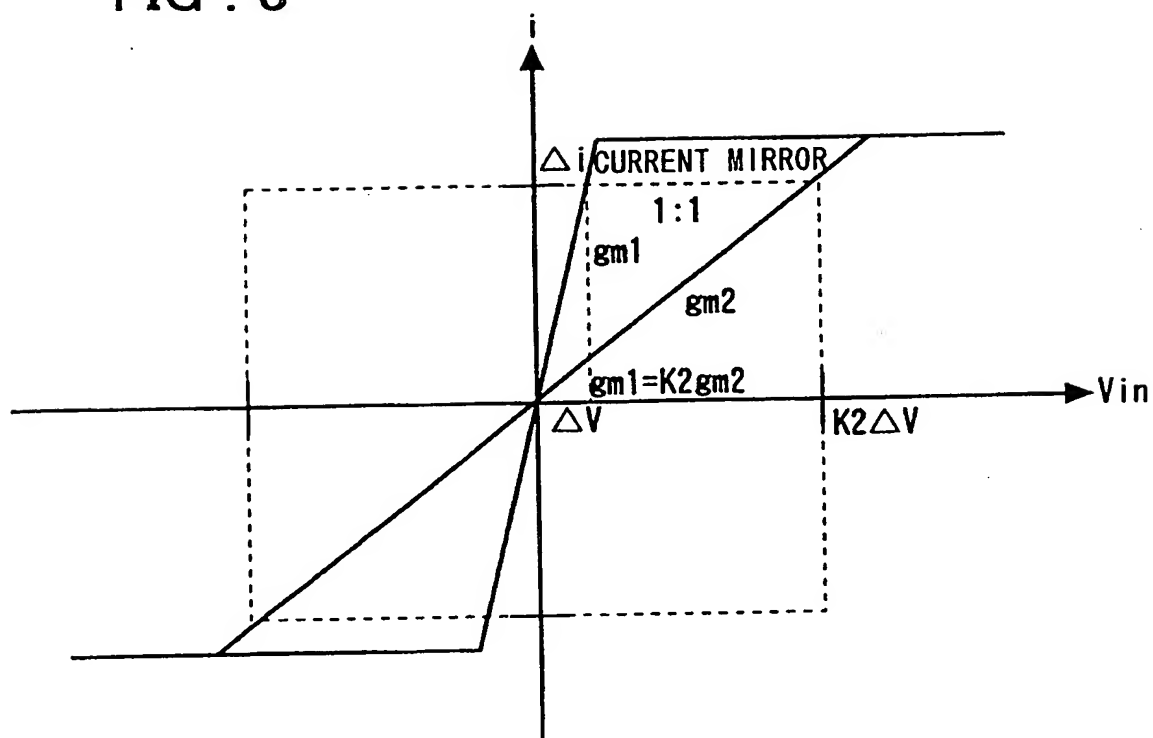
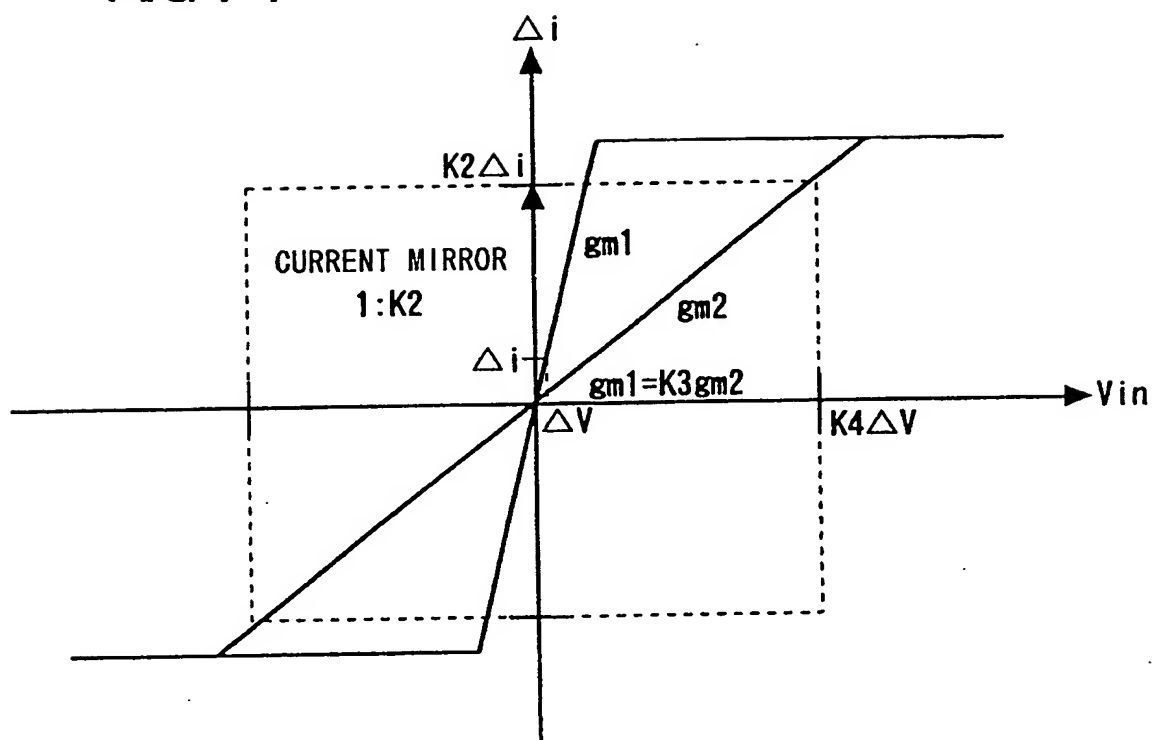


FIG . 4



The circuit diagram shows a multi-stage CMOS amplifier. The input stage consists of a PMOS transistor MP2 and an NMOS transistor MN01, with gain factor K1. The output of the first stage is connected to a second stage consisting of a PMOS transistor MP3 and an NMOS transistor MN02, with gain factor K2. This second stage is followed by a third stage consisting of a PMOS transistor MP4 and an NMOS transistor MN03, with gain factor K3. The output of the third stage is connected to a fourth stage consisting of a PMOS transistor MP5 and an NMOS transistor MN04, with gain factor K4. The output of the fourth stage is connected to a fifth stage consisting of a PMOS transistor MP6 and an NMOS transistor MN05, with gain factor K5. The output of the fifth stage is connected to a sixth stage consisting of a PMOS transistor MP7 and an NMOS transistor MN06, with gain factor K6. The output of the sixth stage is connected to a seventh stage consisting of a PMOS transistor MP8 and an NMOS transistor MN07, with gain factor K7. The output of the seventh stage is connected to a differential output stage consisting of two NMOS transistors MN08 and MN09, with gain factor K8. The differential output is taken from the sources of MN08 and MN09. The circuit is biased by a current source I0 and a reference voltage VREF. The PMOS transistors are labeled MP(K2+4) and the NMOS transistors are labeled MN(2K2+1). The circuit is powered by VDD and ground.

FIG . 7

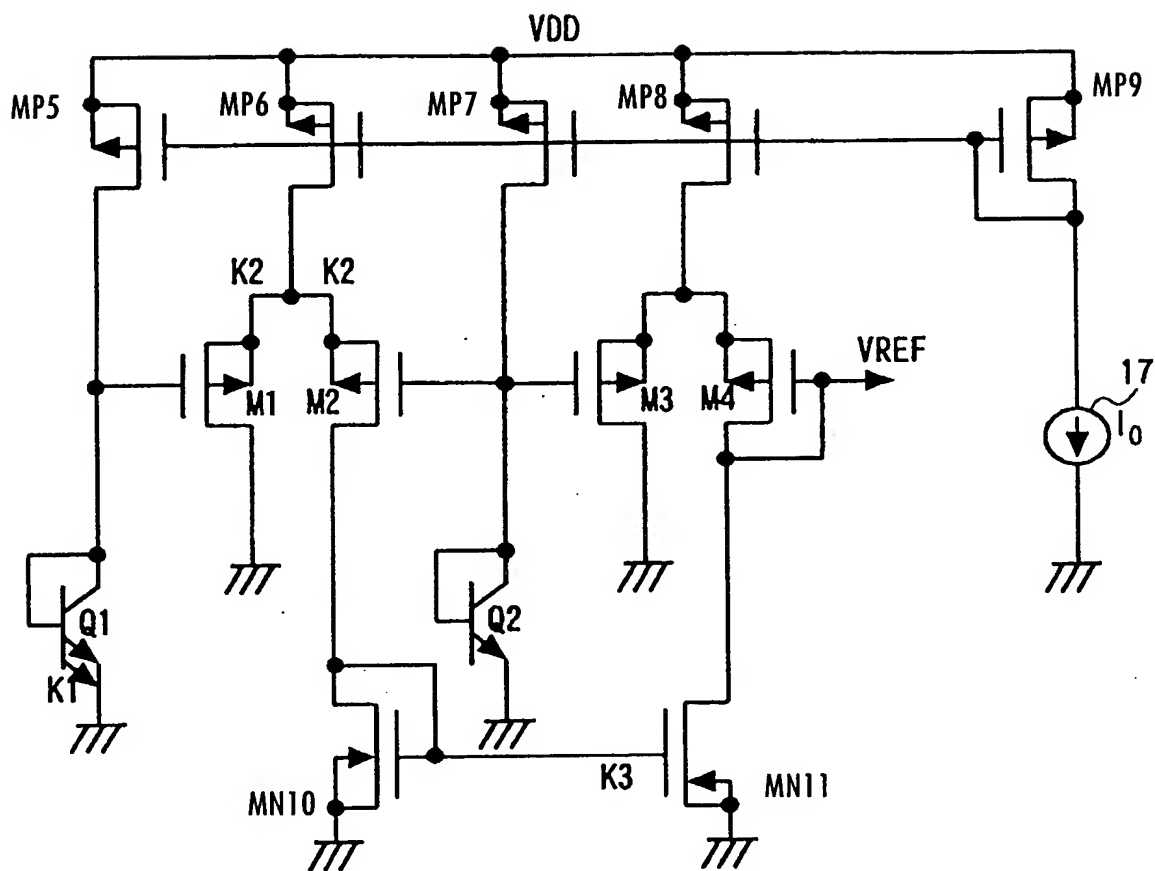


FIG. 8

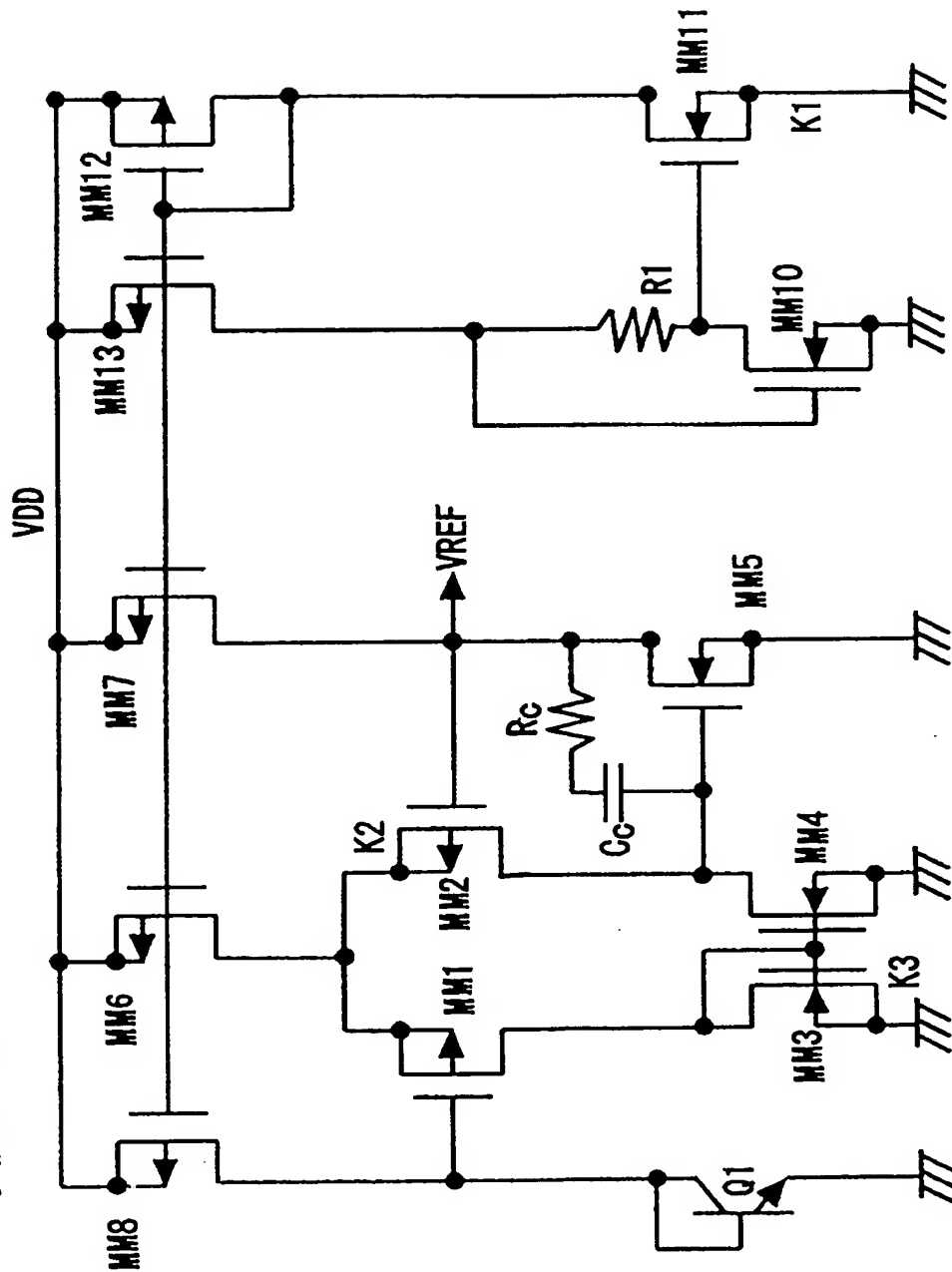


FIG. 9

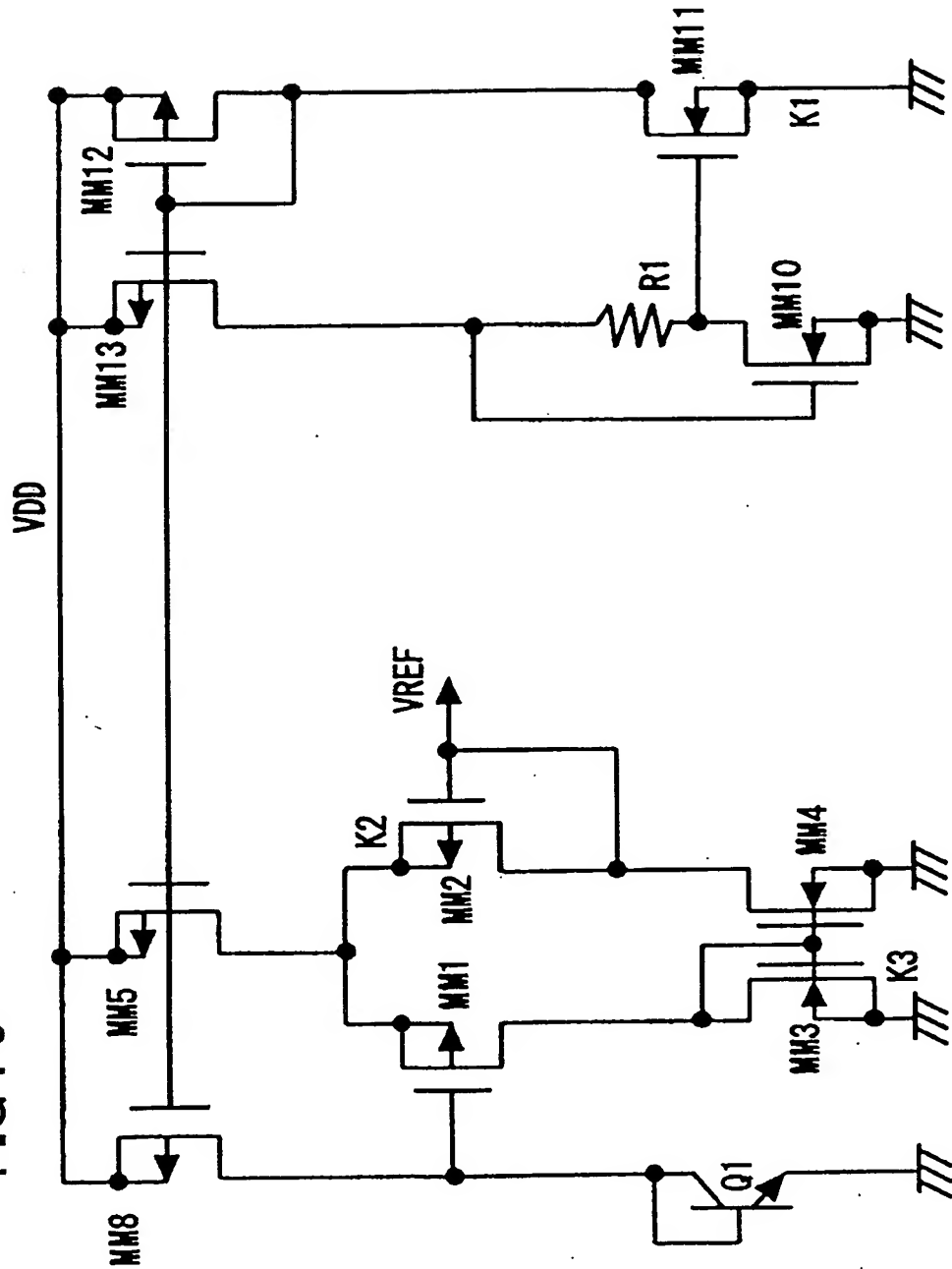


FIG . 10 PRIOR ART

